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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/712,902	11/15/2000	Seong-Rak Choi	5000-1-155	5256
33942	7590	03/17/2004	EXAMINER	
CHA & REITER, LLC 210 ROUTE 4 EAST STE 103 PARAMUS, NJ 07652			MAIS, MARK A	
			ART UNIT	PAPER NUMBER
			2664	
DATE MAILED: 03/17/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/712,902

Applicant(s)

CHOI, SEONG-RAK

Examiner

Mark A Mais

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-11 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-6 is/are allowed.
- 6) ☒ Claim(s) 7-11 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 November 2000 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 6 mailed on 4/4/03.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Priority***

1. Acknowledgement is made of the claim for foreign priority under 35 U.S.C. 119(a)-(d), and receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Information Disclosure Statement***

2. The information disclosure statement (IDS) submitted on April 4, 2003 was filed after the mailing date of the Application on November 15, 2000. The submission is in compliance with the provisions of 37 CFR 1.56 and 1.97. Accordingly, the examiner considered the information disclosure statement.

### ***Drawings***

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Specification***

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means"

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and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because it is longer than 150 words. Correction is required. See MPEP § 608.01(b).

### ***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by Castellano (USP 6,690,670).

8. With regard to claim 7, Castellano discloses a system for accommodating additional subscribers in an ATM system, comprising: a hybrid control means (**Fig. 4c, Device 10**) for transporting ATM traffic (**Fig. 4c, Device 12b**) over a plurality of physical channels (**Fig. 4c, Physical Layer Devices 1 through n**), said physical channels having different fixed bandwidth allocations; a first bandwidth control structure (**Fig. 4c, UTOPIA device 11a**) for directing a first physical channel having a first fixed bandwidth allocation (**155/622 Mbps, col. 2, line 50**); a second bandwidth control structure (**Fig. 4c, UTOPIA device 11b**) for directing a second physical channel having a second fixed bandwidth allocation (**25/50 MHz, col. 3, lines 57-59**) to a plurality of extension boards (**col. 5, lines 4-6**), wherein the first fixed bandwidth allocation is greater than the second fixed bandwidth allocation (**155/622 Mbps > 25/50 Mbps**).

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Castellano as applied to claim 7 above, and further in view of Rich (USP 6,452,927).

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10. With regard to claims 8-9, Castellano does not specifically disclose that the first bandwidth control (**Fig. 4c, UTOPIA device 11a**) structure comprises a subscriber board for interfacing with a switch link (**Fig. 4c, UTOPIA device 11a interfacing with the link between it and the ATM Device 12a**) and for multiplexing/demultiplexing the cell received therein to one of the extension subscribers or that the second bandwidth control structure comprises a means for multiplexing/demultiplexing the data exchanged with the first bandwidth control structure.

Moreover, Castellano does not specifically disclose a first bandwidth control structure (1) which serializes the data prior to transmission to the low-speed device via low-speed serial data exchange (multiplexing) (2) a second bandwidth control structure which recovers the serialized data and converting it back to parallel data for delivery to the low-speed subscriber device (demultiplexing) and, (3) for data flow from the low-speed subscriber device to the ATM switch, serializes the data for transmission (multiplexing) back to the first bandwidth control means for ATM transmission (demultiplexing). However, the Rich reference discloses a rack-mounted architecture that supports physical layer and ATM layer devices (**col. 2, line 43-46**). More importantly, Rich discloses an extender circuit, which provides a serial communication interface between an ATM layer device and a physical layer device (**col. 3, lines 38-41**). Thus, simply put, the circuit converts parallel data to serial data for transmission over the serial communication interface and restores the data to parallel data before either the ATM layer device or the low-speed subscriber device uses it (**col. 3, lines 50-65**). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have serialized the transmission of data over a serial communication line because such a modification eliminates cross-talk and skew problems associated with high speed parallel buses common to ATM

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parallel buses (**col. 6, lines 47-51**) as well as reducing clutter on the rack in and around the ATM switch (**col. 6, lines 51-59**). Since, Castellano discloses a stackable switch system, it would have been obvious that the extension boards for the low-speed devices could be on another shelf within the rack architecture.

11. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Castellano and Rich as applied to claim 9 above, and further in view of Holden et al. (USP 6,147,997).

12. With regard to claim 10, Castellano does not specifically disclose that the second bandwidth control structure further comprises a plurality of extension boards for exchanging data with the multiplexing/demultiplexing means via a low-speed bus and for transmitting the data received therein to one of the subscribers. However, Holden et al. discloses the use of a backplane containing multiple buses serving one or more physical devices (**Fig 2, backplane 230; see also col. 5, lines 5-16**). The UTOPIA 2 standard also delineates the standard bus and protocol for communicating data between the ATM switch and physical layer devices. Holden et al. discloses that the communications data (**address, data, and control information or any combination**) is sent through the bus in the backplane (**col. 3, lines 62-64**). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a bus to control the extension boards because the bus is necessary for controlling the parallel-to-serial-to-parallel conversions as well as the multiplexing/demultiplexing such that the correct cells reach the correct physical devices and transmit the correct cells to the ATM switch. Moreover, it allows

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the stacked architecture of the ATM rack to maintain a convenient line card design (**col. 3, lines 3-5**).

13. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Castellano as applied to claim 7 above, and further in view of Chung et al. (USP 6,487,203).

14. With regard to claim 11, Castellano does not specifically disclose that the data being exchanged between the first and second bandwidth control structures include a PBA ID (Physical Block Address Identification) for identifying one of the extension boards, a link number for identifying the low-speed subscriber link, and a UDF (User Define Function) data. Utopia Level 2, Version 1.0 discloses the ATM Forum's cell format (**page 8, Figure 2.4**). Chung et al. has changed the format to include the physical device's groups (PBA ID), physical port number (link number) and a UDF to allow the system to use 64 ports instead of 31 as defined in UTOPIA 2 (**col. 2, lines 19-24**). Chung et al.'s cell also allows for a multiplexed polling of more ports than was originally disclosed for UTOPIA 2. Thus, it would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the standard UTOPIA cell to include the block address, link number, and UDF because such a modification allows an ATM rack to include a second stack of extension boards for low-speed subscriber devices and because the management of the extension boards and their links is essential to making the communication/transmissions work successfully between the ATM switch and the low-speed UTOPIA device connected to an extension board.



***Allowable Subject Matter***

15. Claims 1-6 are allowed.

16. The following is a statement of reasons for the indication of allowable subject matter:

The Examiner has not found a system for extending capacity to accommodate low-speed UTOPIA-2 subscribers in an ATM switching system comprising: (1) a subscriber board interfaced with a switch link via a system backboard which receives cells from the switch link and multiplexes/demultiplexes the received cells via a UTOPIA interface after performing an ATM layer operation; (2) a physical layer board which exchanges data with the lower-speed subscriber by serializing the cells transmitted from the subscriber board into a clock and data bits for transmission to the low-speed subscriber; (3) a multiplexing/demultiplexing board which receives the serialized clock and data bits from the physical layer board via a cable, and makes a serial-to-parallel conversion of the serialized cells into a word unit, multiplexes the read cells, and transmits the multiplexed read cells to the physical layer board via a link processor; and (4) a plurality of extension boards which exchange cells with the multiplexing/demultiplexing board via a low-speed bus, performs physical layer operations on the received cells, and transmit the received cells to the correct low-speed subscriber via the physical layer board.

***Conclusion***

17. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

(a) Holden et al. (USP 6,188,690) Method and apparatus for high-speed, scalable communication system.

(b) Yamanaka (USP 6,693,911) Asynchronous transfer mode apparatus.

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(c) UTOPIA Level 1, Version 2.01 (af-phy-0017.000), March 21, 1994.

(d) Byers (USP 5,781,320) Feier Access Architecture. Discloses line cards connected, inside of customer premises equipment over a 622 Mbps switch link.

(e) Chin et al. (USP 6,343,077) Stacking Utopia Switching.

(f) Cole (USP 5,956,344) Interprocessor communications in ATM environment.

Discloses using inter-processor communications in an ATM environment where, within a distributed memory multiprocessor architecture, inter-processor communication is performed by passing messages.

(g) Lau et al. (USP 6,356,561). Lau et al. discloses arbitrating several physical layer devices on a round-robin basis.

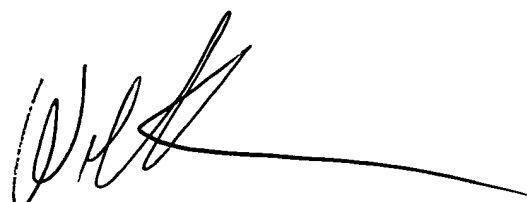
18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A Mais whose telephone number is (703) 305-6959. The examiner can normally be reached on 8:00-4:30.

19. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on (703) 305-4366. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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20. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 20, 2004



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